IN THE CLAIMS

Please amend the claims as follows:

1.   (Withdrawn) A computer processor comprising

a plurality of functional units, where each functional unit is coupled to a
      register file for reading and writing operands;

an instruction fetch unit coupled to receive instructions from a memory system;

an instruction decode and dispatch unit coupled to the instruction fetch unit for
      receiving instructions therefrom and coupled to the functional units to
      dispatch commands to the plurality of functional units;

a resource status flags register wherein particular functional units may be
      marked enabled or disabled for use;

wherein the instruction fetch and decode unit checks the resource status flags
      register prior to dispatching commands and dispatches commands only
      to those functional units marked enabled in the resource status flags
      register;

and wherein the instruction fetch and decode unit is capable of stalling if
      insufficient resources are available, and of dispatching remaining
      commands in a following cycle.

2.   (Withdrawn) The computer processor of Claim 1, wherein the
resource status flags register is implemented with programmable memory cells
capable of being programmed at factory test.

3.   (Withdrawn) The computer processor of Claim 1, wherein the
plurality of functional units includes a plurality of integer units, and wherein the
computer processor is capable of executing integer instructions if at least one
integer unit of the plurality of integer units is marked enabled in the resource status
flags register.

4.   (Withdrawn) The computer processor of Claim 1, wherein the
plurality of functional units includes a plurality of floating point execution units,
and wherein the computer processor is capable of executing floating point

instructions if at least one floating point unit of the plurality of floating point units is marked enabled in the resource status flags register.

5.   (Withdrawn) The computer processor of Claim 4, wherein the plurality of functional units includes a plurality of integer units, and wherein the computer processor is capable of executing integer instructions if at least one integer unit of the plurality of integer units is marked enabled in the resource status flags register.

6.   (Withdrawn) The computer processor of Claim 5, wherein the plurality of functional units includes a plurality of units capable of fetching operands from memory, and wherein the computer processor is capable of executing load instructions if at least one unit capable of fetching operands from memory of the plurality of functional units is marked enabled in the resource status flags register.

7.   (Withdrawn) The computer processor of Claim 5, wherein at least one functional unit is marked disabled in the resource status flags register.

8.   (Original) A method of selling a partially defective processor integrated circuit comprising the steps of:

     providing a plurality of functional units on the integrated circuit;

     providing a resource status register wherein functional units of the plurality of functional units may be marked with status selected from the group consisting of enabled and disabled;

     testing an integrated circuit to determine which functional units are defective;

     programming the resource status register to mark defective functional units as disabled and remaining functional units as enabled;

     classifying the integrated circuit into bins according to performance available with the enabled functional units;

     packaging the integrated circuit; and

     selling the integrated circuit as capable of performance appropriate for the bin into which it was classified.

9.   (Original) The method of Claim 8, wherein the step of classifying is performed by a table lookup, the table having been prepared based upon benchmark results.

10.   (Original) The method of Claim 8, wherein the functional units include a plurality of integer execution units and a plurality of floating point execution units.

11.   (Currently Amended) The method of Claim 8 10, wherein at least one defective floating point unit of the plurality of floating point execution units is marked disabled and at least one remaining floating point unit of the plurality of floating point execution units is marked enabled.

12.   (Original) The method of Claim 8, wherein a functional unit of the plurality of functional units is a branch prediction unit, and wherein the branch prediction unit is capable of being disabled through programming the resource status bits.

13.   (Currently Amended) The method of Claim 12, wherein at least one defective floating point unit of a plurality of floating point execution units on the partially defective processor integrated circuit is marked disabled and at least one remaining floating point unit of the plurality of floating point execution units is marked enabled.

14.   (Original) A method of selling a partially defective processor integrated circuit comprising the steps of:
        providing a plurality of functional units on the integrated circuit;
        providing a resource status bit associated with each functional unit wherein
                each functional unit of the plurality of functional units may be marked
                with status selected from the group consisting of enabled and disabled;
        testing an integrated circuit to determine which functional units are defective;
        programming the resource status register to mark defective functional units as
                disabled and remaining functional units as enabled;

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classifying the integrated circuit into bins according to performance available

with the enabled functional units;

packaging the integrated circuit; and

selling the integrated circuit as capable of performance appropriate for the bin

into which it was classified.

15.   (Original) The method of Claim 14, wherein the step of classifying is performed by a table lookup, the table having been prepared based upon benchmark results.

16.   (Original) The method of Claim 14, wherein the functional units include a plurality of integer execution units and a plurality of floating point execution units.

17.   (Currently Amended) The method of Claim 14, wherein one the resource status bits are set according to results of built in self test upon powerup of each functional unit.

18.   (New) The method of Claim 14, wherein the resource status bits are implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale.

19.   (New) The method of Claim 11, wherein the resource status register is implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale.

20.   (New) The method of Claim 12, wherein the resource status register is implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale.